

Ethernet Alliance Technical Committee Meeting

October 15, 2013



Agenda

- What's new in BASE-T
- Highlights: 25GBASE-T CFI
- Highlights: Next Generation Enterprise BASE-T CFI
 - Peter Jones



Lot's of Activity in Twisted Pair

Five active projects in 802.3 for Twisted Pair

- P802.3bp 1000BASE-T1
- P802.3bq 40GBASE-T
- P802.3bt DTE Power via MDI over 4-Pair Task Force
- P802.3bu 1-Pair Power over Data Lines Task Force
- P802.3bw 100BASE-T1 Task Force

Two CFIs scheduled for November

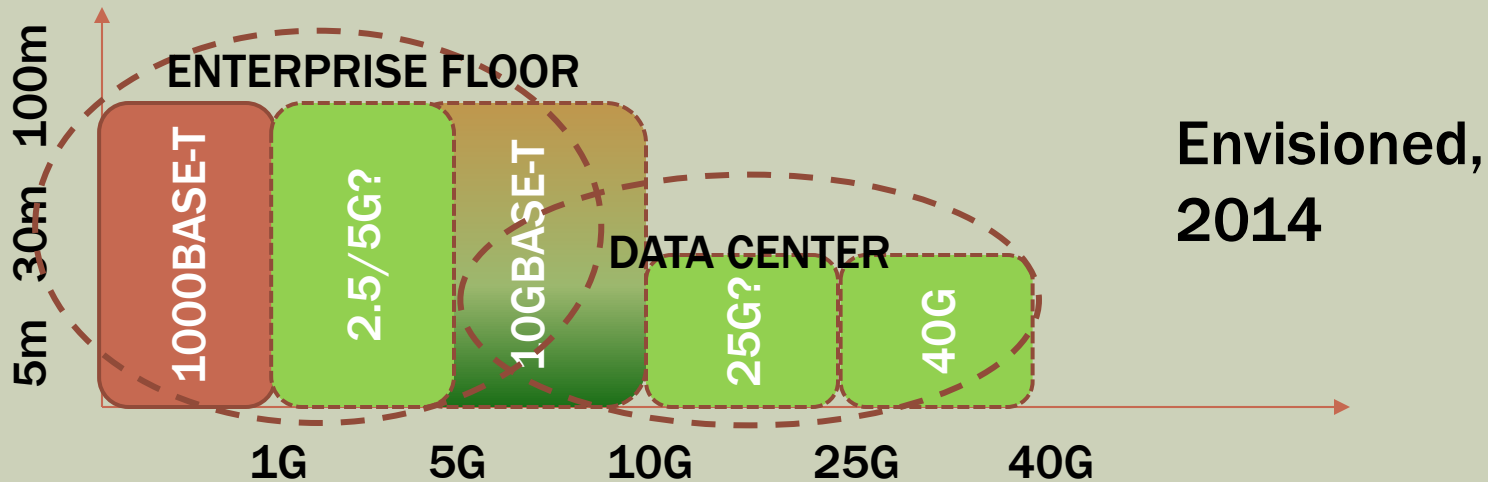
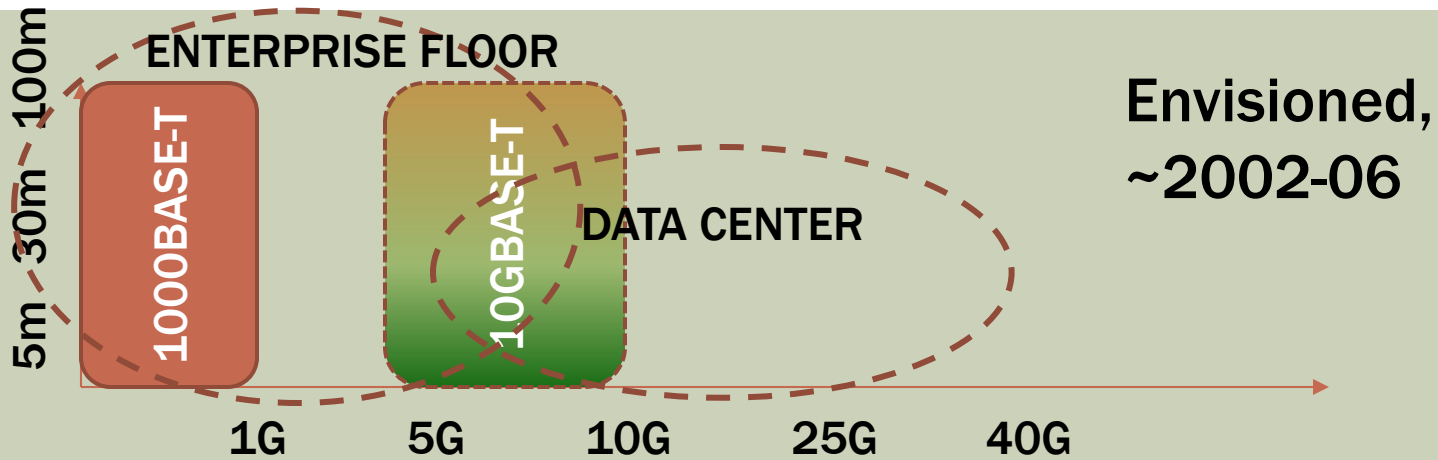
- Next Generation Enterprise Access BASE-T
- 25GBASE-T

- Even Scott Kipp is talking about BASE-T!!



THE CHANGING SPACES OF BASE-T

GEORGE ZIMMERMAN, CME CONSULTING



25GBASE-T CFI Overview



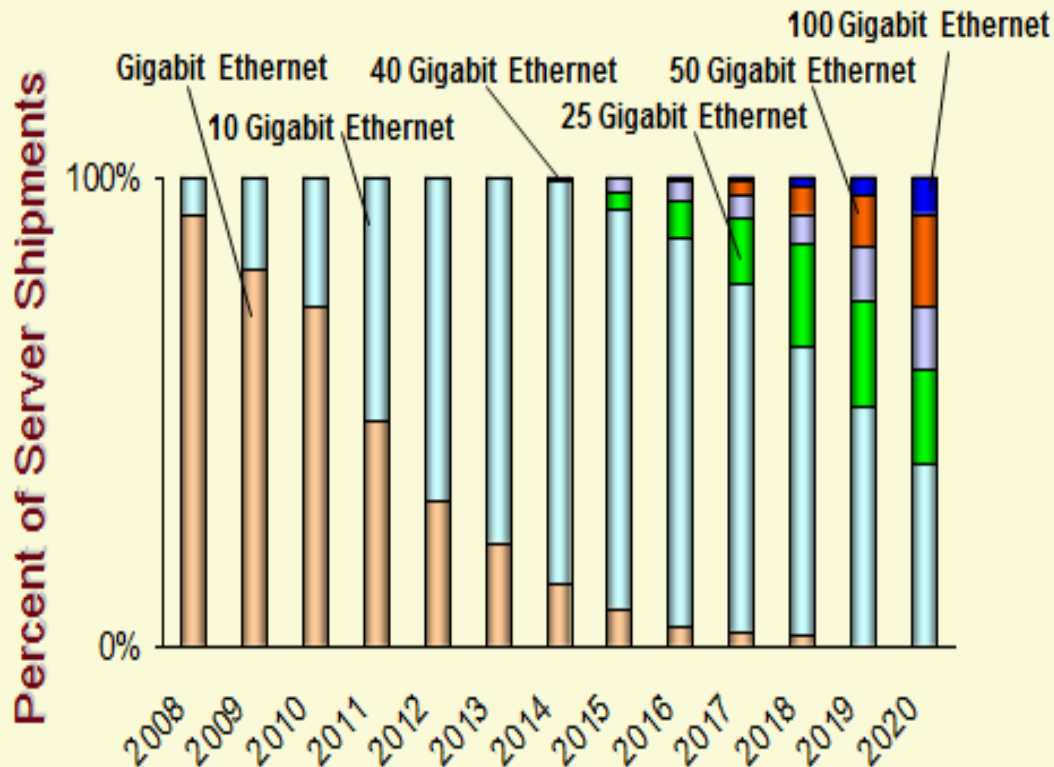
25GBASE-T Market Drivers

- Cloud vs. Enterprise
- Update on server port speed forecast
- Media mix
- Topology
- Cost Optimization



Speed Migration on Cloud Servers

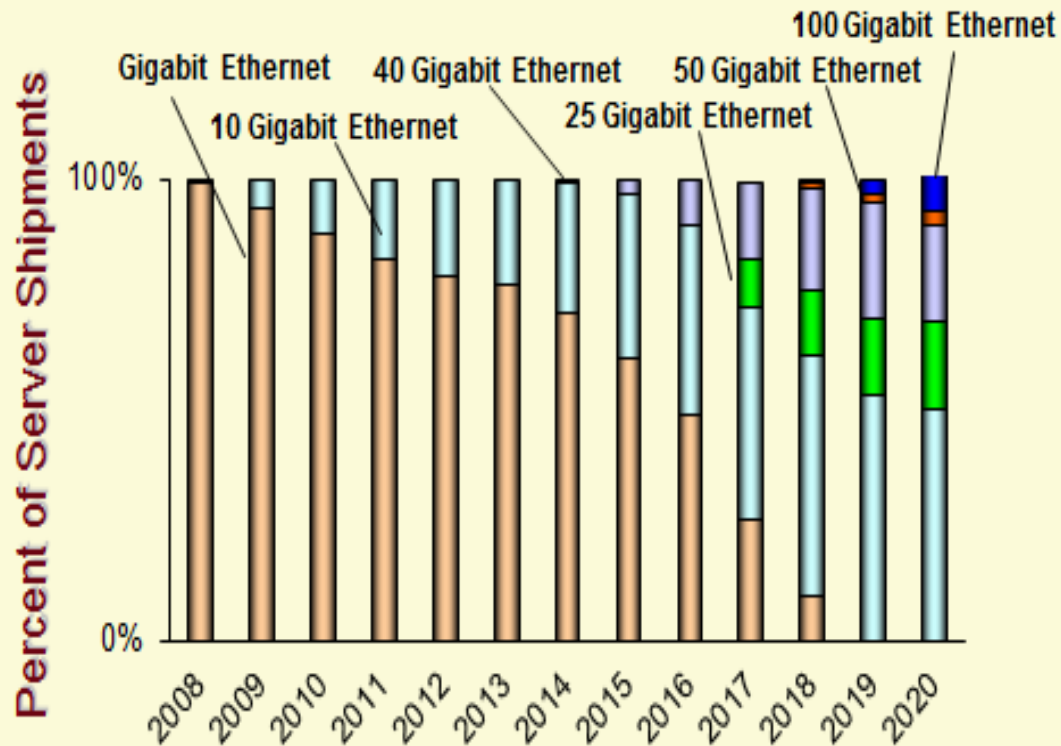
Speed Migration on Cloud Servers (Included in Dell'Oro Group's Server Report)



- ~25% of server shipments today
- Transition to 10G nearly complete
- Early adoption of 40G, but 25G/50G expected to overtake
- Standardization not imperative
 - Engineered systems

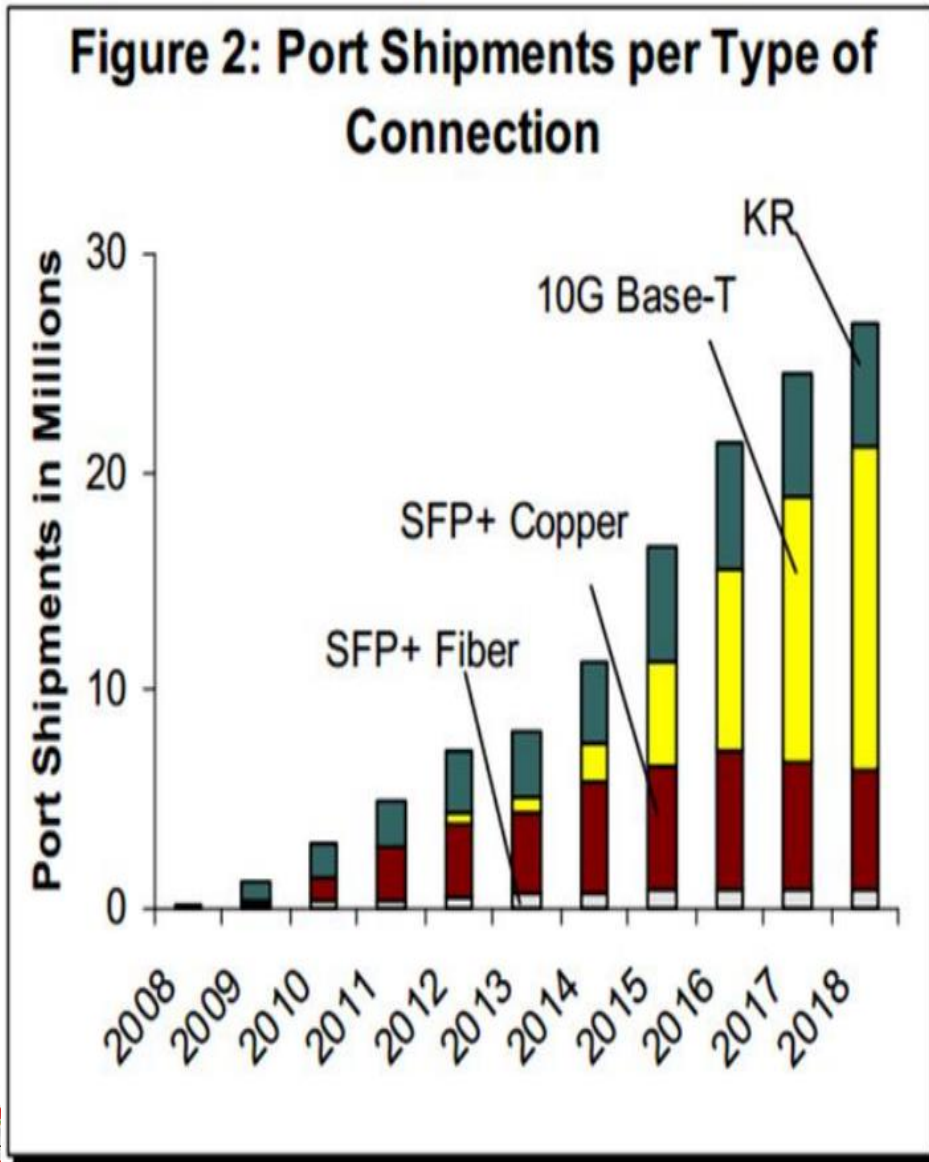
Speed Migration on Premise Servers

Speed Migration on Premise Servers (Included in Dell'Oro Group's Server Report)



- ~75% of server shipments today
- 1000BASE-T still majority of ports
- 10G growing
- Anticipate both 40G and 25G to be deployed
- Largely follow TIA-942, and deploy a variety of access switch placements including MoR and EoR.

10G Server Port Type Mix



- 10G Early Adopters on Fiber, Backplane, and Twinax
- 10GBASE-T grows as 1G → 10G transition progresses in Enterprise

Top of Rack, Middle & End of Row

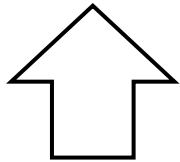
ToR



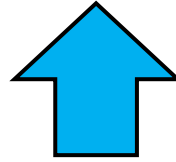
MoR



EoR



Intra-rack can be addressed by 25Gb/s copper direct attach

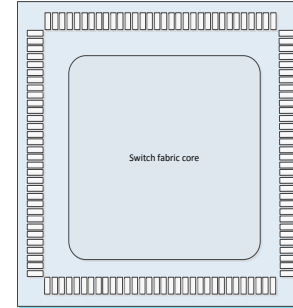


Not addressed by 25Gb/s copper direct attach



25Gb/s I/O Efficiency

- Single 25 Gb/s lane per port connection from switch to PHY maximizes connectivity available in single ASIC
- Switch ASIC Connectivity limited by serdes I/O
- 25Gb/s lane maximizes bandwidth/pin and switch fabric capability vs. older generation
- 25Gb/s port optimizes both port count and total bandwidth for server interconnect



For a 128 lane switch:

Port Speed (Gbps)	Lane Speed	Lanes /port	Usable ports	Total BW (Gbps)
10	10	1	128	1280
25	25	1	128	3200
40	10	4	32	1280
40	20	2	64	2560
100	25	4	32	3200

Using 25Gb/s ports maximizes connectivity and bandwidth.

Feasibility Comparison

Parameter	10GBASE-T (ref- Cl55)	40GBASE-T (ref- Cl 98d1.0)	25GBASE-T (example)
Channel	100m, Cl 55.7	30m, Cl 98.7	30m, Cl 98.7
Baud (MHz)	800	3200	2000
RX_ENOB (bits)	10	7.8	6.5
Channel round trip (baud)	880	1056	660
Echo Cancellation (dB)	55	47 (-6dB) to 55	43 (-12dB) to 55
NEXT Cancellation (dB)	40	34 (-6dB) to 40	28 (-12dB) to 40
FEXT Cancellation (dB)	25	22 (-3dB) to 25	19 (-6dB) to 25
Relative Margin w/same ADC_pwr_factor	0 (ref)	+2.7dB to 0.2 dB	+8.7dB to +4dB

Better than existing projects on most parameters



Potential Path Forward

- After CFI, Study Group creates project documentation to add 25GBASE-T to P802.3bq
- Sep'14: Request CFI prior to Sept 29th (Done)
- Nov'14: Hold CFI at 802.3 plenary
 - motion in 802.3 to form Study Group at closing
- Jan'15: Hold SG mtg to modify PAR & CSD,
 - to be forwarded 30 days before March plenary
- Mar'15: 802.3 approval of changes; higher layer approvals
- May'15: P802.3bq operates with expanded scope

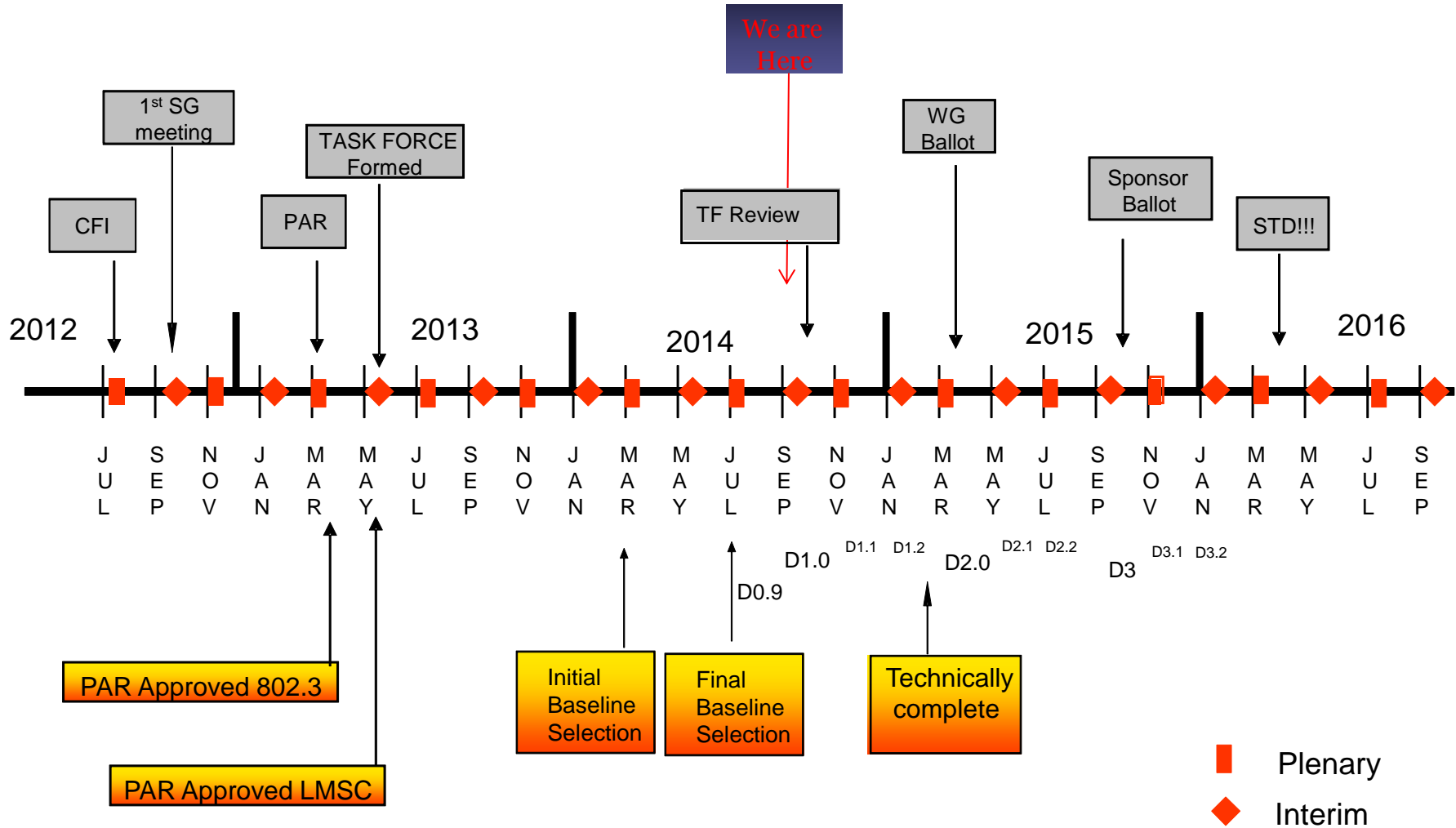


Considerations

- A CFI and Study Group are necessary for 802.3
 - That's the process...
- Main SG task: Determine reach & channel objectives
 - 30m Cat8 likely (same as 40GBASE-T)
 - Can any legacy cabling be supported?
- Impact to P802.3bq project timeline is likely small
- If bq has already in WG ballot, expanded scope will allow necessary mods to draft
- Need time for 25G to enter TF phase and set architecture direction



P802.3bq Adopted Project Timeline



Call to Action

- Review the complete CFI Consensus Presentation
- Express your support
- Email me if you need the deck, and to comment.
 - David.chalupsky@intel.com

