OIF CEI-56G Project Activity

Progress and Challenges for Next Generation 400G Electrical Links

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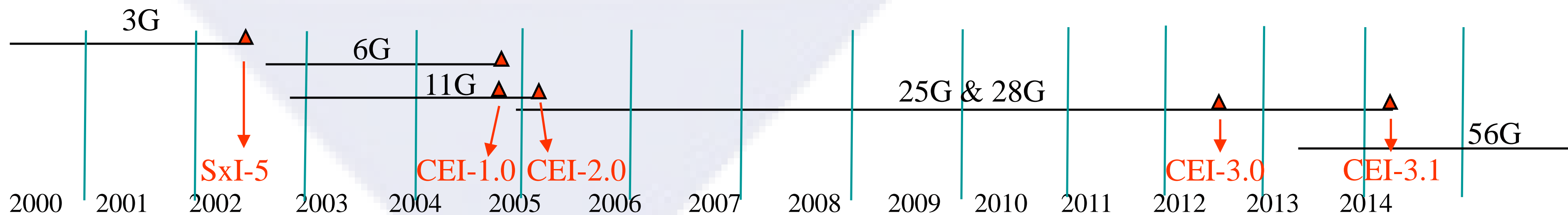
Electrical Implementation Agreements

- CEI IA is a clause-based format supporting publication of new clauses over time:
  - CEI-1.0: included CEI-6G-SR, CEI-6G-LR, and CEI-11G-SR clauses.
  - CEI-2.0: added CEI-11G-LR clause
  - CEI-3.0: added work from CEI-25G-LR, CEI-28G-SR
  - CEI-3.1: will add CEI-28G-MR and CEI-28G-VSR
- CEI-11G and -28G specifications have been used as a basis for specifications developed in IEEE 802.3, ANSI/INCITS T11, and IBTA.
- CEI 56G projects are in progress:
  - MR: chip to chip
  - VSR: chip to module
  - XSR: chip to optics engine (separate chips)
  - USR: chip to optics engine (2.5D or 3D package)



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CEI-25G Application Space

CEI-28G-VSR

Chip → Optics → Optics → Chip

Chip-to-Optics

CEI-28G-SR

Chip → Chip

Chip-to-Chip (300 mm)

CEI-28G-MR

Chip → Chip

Low loss Backplane (500 mm)

CEI-25G-LR

Chip → Chip

Backplane (700 mm) or
Passive Copper Cable

Published in CEI 3.0:

- LR: Backplane, passive copper cable.
- SR: Chip-to-chip, and chip-to-module.

Published in CEI 3.1:

- MR: Chip-to-chip, and low loss backplane.
- VSR: Chip-to-module (fully retimed optics)

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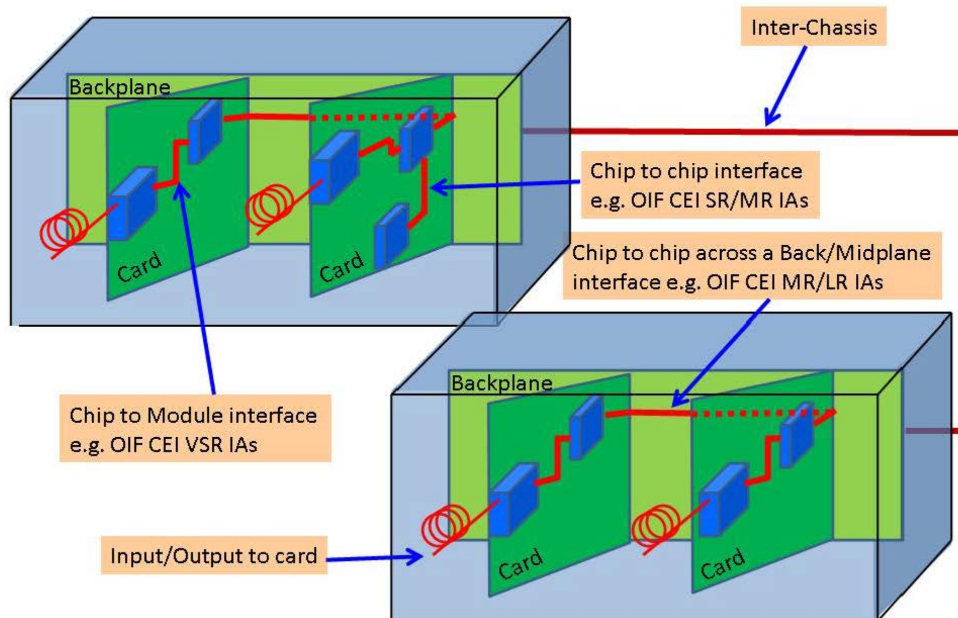
Next Generation Progress Toward 400G

- "OIF Next Generation Interconnect Framework" white paper lays out a roadmap for OIF electrical and optical projects to support next generation interconnects.
- CEI-56G electrical track projects were started in the Physical & Link Layer Work Group based on the white paper.
- Technical contributions have been submitted and debated. These include but are not limited to:
  - Investigations of PHY chip requirements and technology
  - Investigations of Serdes roadmaps
  - Power trade-off investigations
  - Alternate signaling investigations
- These efforts now enable the OIF to establish paths forward.
  - Target to adopt baseline technical proposals this year.
  - Target to publish CEI IAs by the end of 2015.
- The following charts describe the application spaces that have emerged for CEI-56G, and the challenges and trends that are emerging from this work.

CEI Application Space is Evolving

- The "OIF Next Generation Interconnect Framework" white paper lays out a roadmap for CEI-56G serial links.
  - 2.5D and 3D applications are becoming increasingly relevant.
  - High function ASICs (such as switch chips) are driving requirements for higher I/O density and lower interface power.
  - Chip-to-chip and mid-plane interfaces are becoming more relevant than high loss backplanes (at least in the near-term).



- Overall themes emerging:
  - Pin density is not increasing fast enough for high density ASICs.
  - Power reduction of 30% from one generation to next is not good enough.

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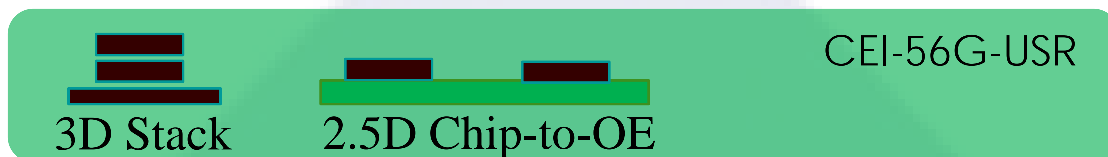
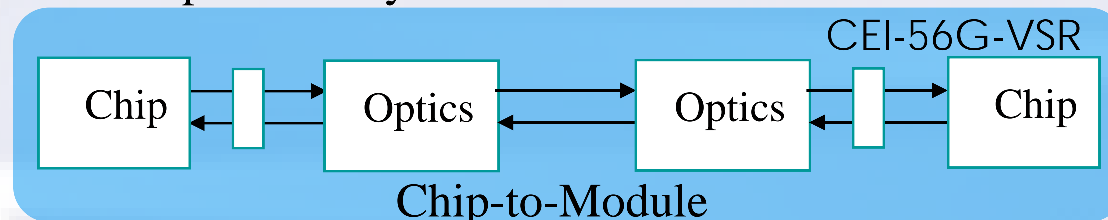
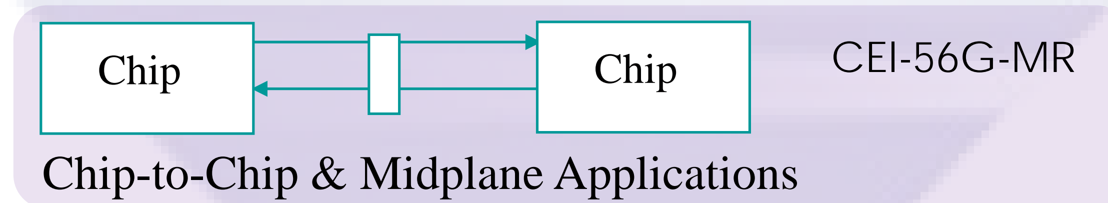
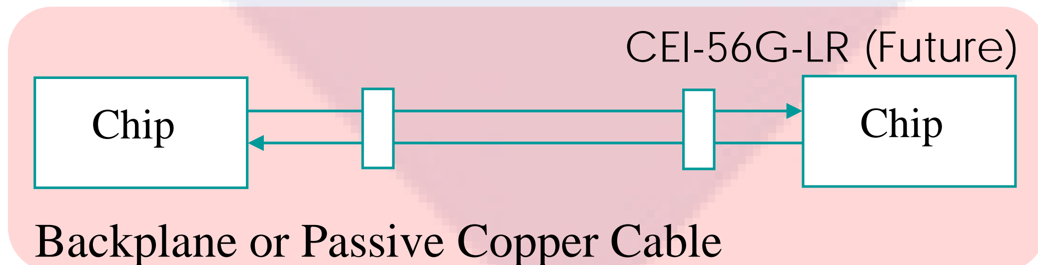
CEI-56G Application Space









CEI-56G Application Space:

- MR: Interfaces for chip to chip and midrange backplane.
  - 50 cm, 1 connector
  - 15-25 dB loss @14 GHz
  - 20-50 dB loss @28 GHz
- VSR: Chip-to-module
  - 10 cm, 1 connector
  - 10-20 dB loss @28 GHz
- XSR: Chip to nearby optics engine.
  - 5 cm, no connectors
  - 5-10 dB loss @28 GHz
- USR: 2.5D/3D applications
  - 1 cm, no connectors, no packages

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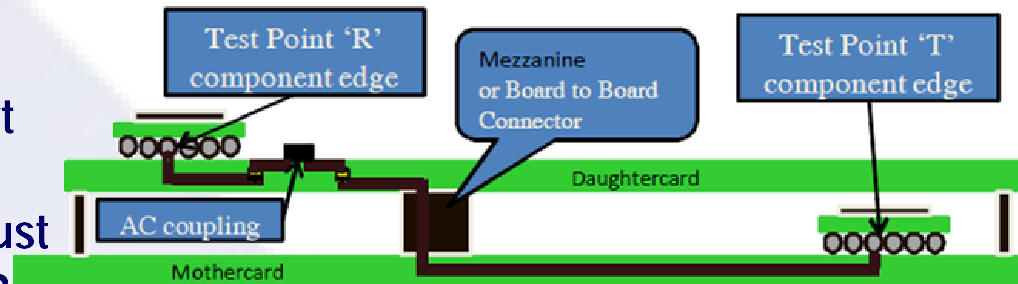
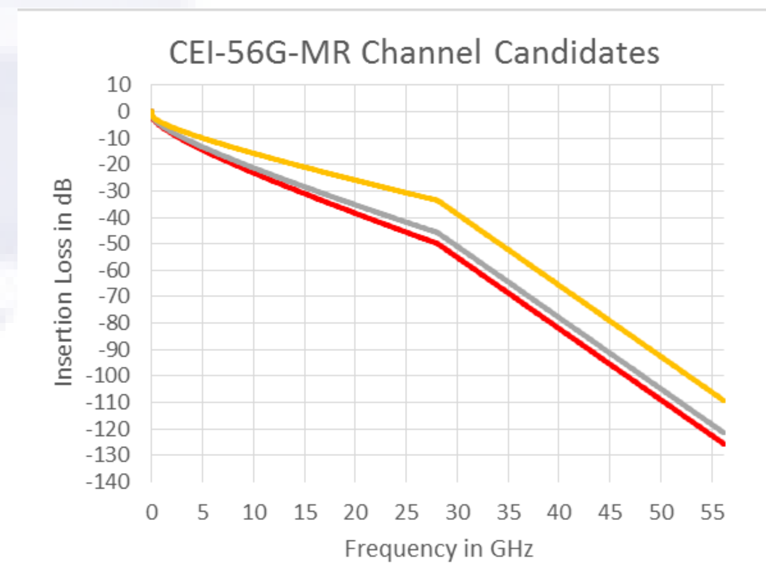
CEI-56G Medium Reach (MR)

- Chip-to-chip standards must operate at 56 Gb/s to support 2-lane OTU-4 i/f.
- Chip-to-chip applications must budget for 20 inches of reach and 1 connector.
- Channel insertion loss of 15-25 dB @14 GHz
  - 28G-MR IL = 20dB @14GHz
  - Not expected to improve much for CEI-56G.
- Consensus emerging that 56 GBd NRZ is not a viable option for the MR channel.
  - PAM-4 or other advanced signaling is needed.
  - NRZ limitations are also driving interest in lower baud rates (40 GBd).





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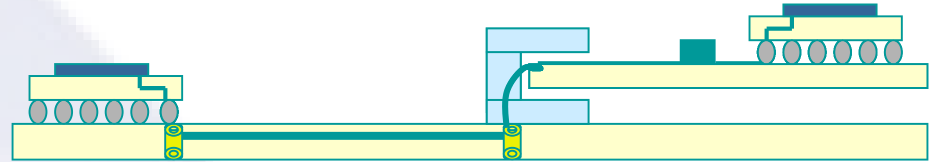
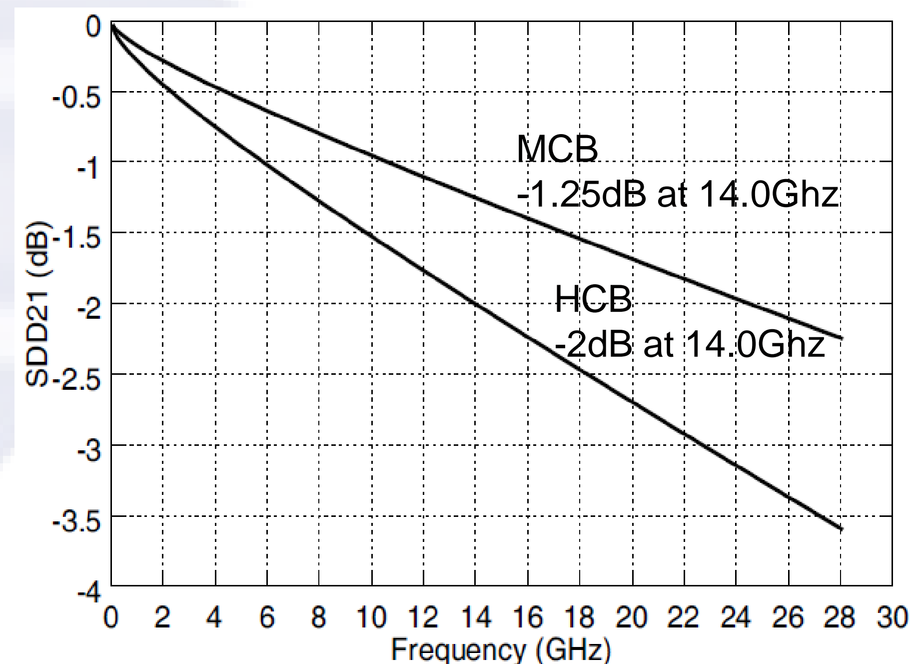
CEI-56G Very Short Reach (VSR)

- Chip-to-module standards must operate at 56 Gb/s to support 2-lane OTU-4 i/f.
- Chip-to-module applications must budget for 6 inches of reach with 1 connector.
- VSR specifies Tx and Rx parameters at the connector compliance point
  - This is different from other CEI variants, which specify compliance at chip balls.
- Both 56GBd NRZ and 28GBd PAM-4 are viable signaling technologies for VSR channels.
  - Selecting NRZ would raise potential compatibility issues with CEI-56G-MR.





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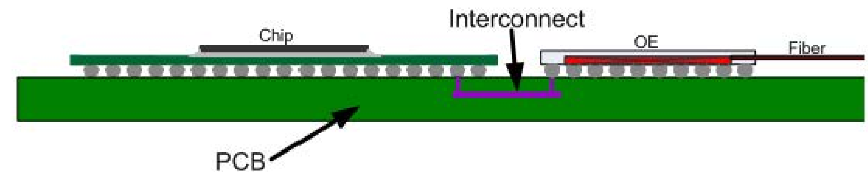
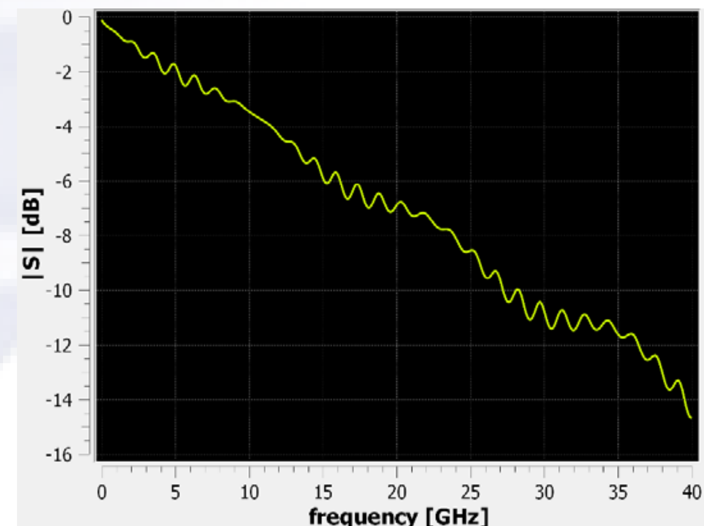
CEI-56G Extra Short Reach (XSR)

- Chip-to-OE standards must operate at 56 Gb/s to support 2-lane OTU-4 i/f.
- Chip-to-module applications must budget for 5 cm of reach with no connectors.
- Application is being driven by large switch chips interfacing to nearby PHY function chips (electrical or optical):
  - Pin density is not increasing fast enough to support next generation switch chips.
  - Interface power is not decreasing fast enough.



Sdd21 for Channel+Packages



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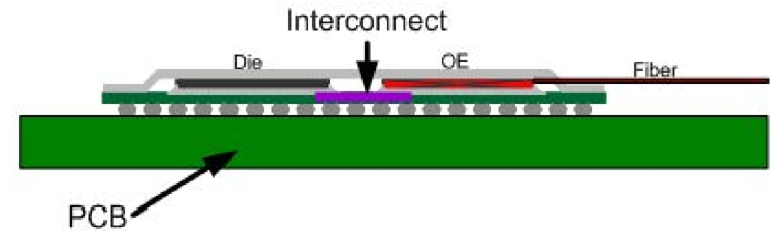
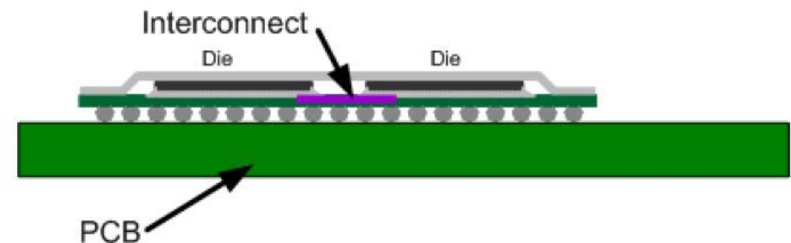
CEI-56G Ultra Short Reach (USR)

- Chip-to-OE standards must operate at 56 Gb/s to support 2-lane OTU-4 i/f.
- Applications must budget for 1 cm of reach with no connectors and with no packages.
- Applications:
  - Chip to Optics Engine interface over silicon substrate.
  - Chip to memory interface over silicon substrate.
  - Chip to chip interface where function has been split across multiple die.
- A narrow interface is desired for chip-to-OE applications; other applications may be much wider.
- Pin density and power is particularly important to applications with wide interfaces.





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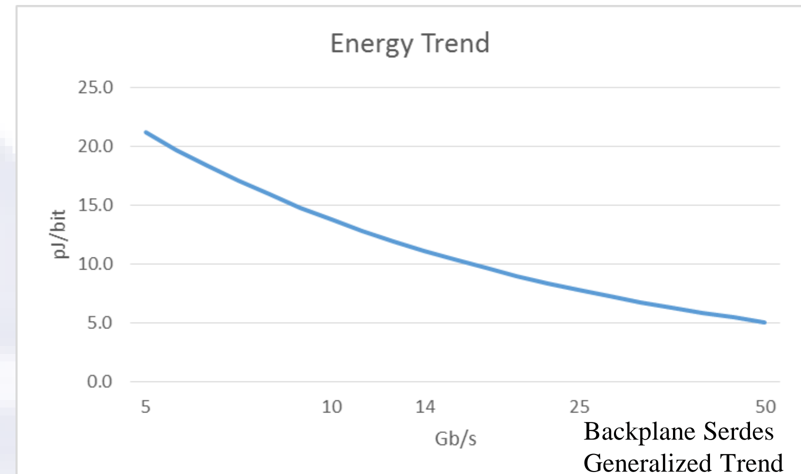
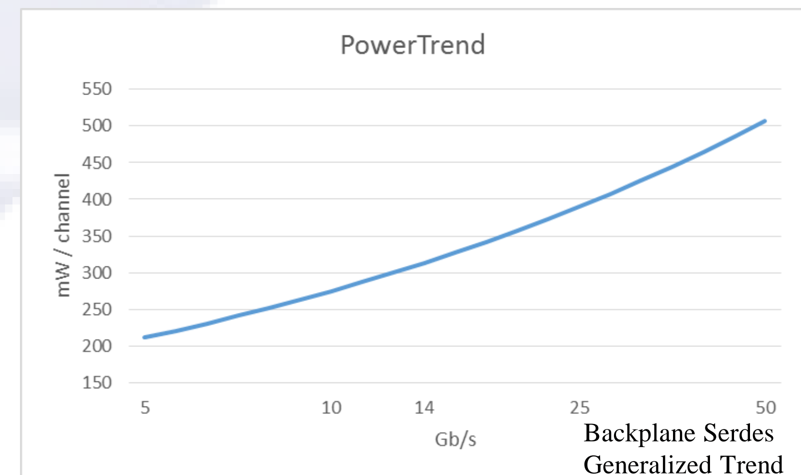
400G Density Challenges

- As interface speeds increase, bandwidth density must increase proportionally to maintain the value proposition.
  - Number of interface wires to/from the optics module affects physical dimensions and faceplate real estate.
- 100G Ethernet was initially specified using existing 10Gb/s electrical link technology which hindered adoption, and is now migrating to 25Gb/s electrical link technology.
  - Ten 10Gb/s links required per direction => 40 wires for a full duplex lane.
  - Faceplate density for early 100G systems was worse than 10G systems.
  - Four 25Gb/s links reduces wire count => 16 wires for a full duplex lane.
- Faster migration path is needed for 400Gb/s Ethernet:
  - Early specifications might assume sixteen 25Gb/s links => 64 wires; but this would limit deployment.
  - Migration path to eight 50Gb/s links will be necessary to facilitate widespread adoption => 32 wires.
- Reducing I/O counts also reduces power requirements. Power dissipation remains a significant system design issue.

Power Challenges

- As baud rates increase, energy per bit trends downward while overall power per channel trends upward.
  - Each doubling of baud rate results in about 30% less power per bit.
  - Reduction in pJ/bit largely driven by process technology node migration.
  - In the future, process migration may not be sufficient to sustain similar reductions.
- System port density remains constant, and therefore power trend drives system power upward.
  - Power/cooling requirements on system are exceeding ability to air cool racks.
  - Methods to break the historical trend and flatten power increases are needed.
- Power consumption of the internet is becoming a significant portion of the planet's energy production.





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Market Bifurcation

- Application space for prior generations consisted of SR, VSR, MR, LR applications.
  - Similar signaling solution was used for the entire range of applications.
  - Common Serdes design was often used, especially on early products.
- Chip power limitations for large ASICs is forcing LR/MR Serdes function off chip.
  - Signaling for MR/LR may be different from lower loss applications.
  - Substantially different Serdes designs with substantially reduced power requirements are required for USR/XSR applications as compared to MR/LR applications.

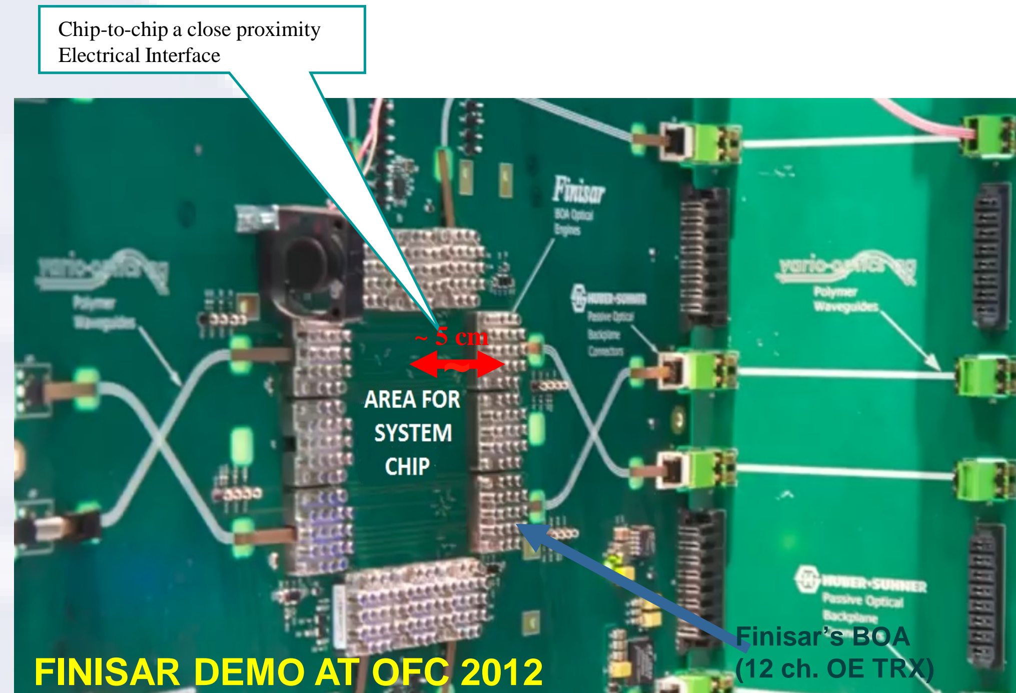

Photo Source: Close Proximity Electrical Interface Project Start

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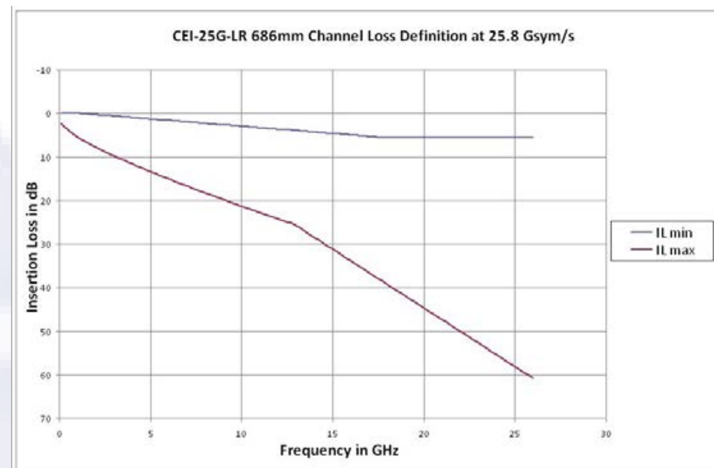
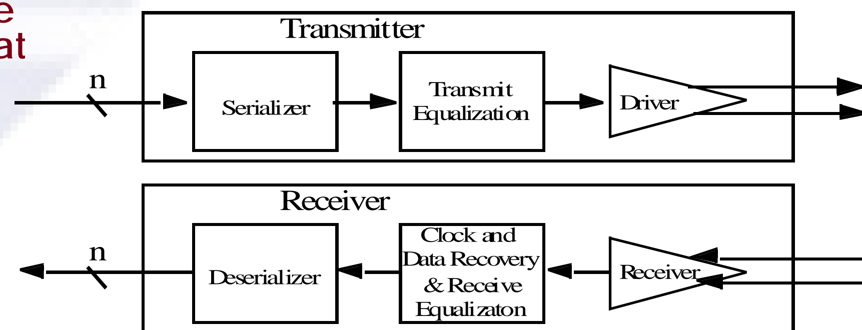
Signaling and Channel Challenges

- Achieving 25 Gb/s was accomplished through evolution in *both* Serdes *and* channel technology.
  - NRZ FFE/DFE architecture evolved to add CTLE and FEC.
  - Better connector technology emerged.
  - Better backplane design and manufacturing techniques became common practice.
- Advanced signaling will likely be required for MR/LR applications at 56 Gb/s.
  - NRZ not viable at losses above 36 dB.
  - Most easily achievable channel design improvements were already deployed to support 25 Gb/s.
  - PAM-4 or other advanced signaling will be needed to support high loss applications at 56 Gb/s and up.
- NRZ is still viable for VSR and lower loss applications.
  - LR/MR will likely adopt PAM-4 or another advanced signaling technique.
  - XSR/USR will likely adopt NRZ signaling.
  - VSR signaling is to be determined.





Summary

- OIF has an established history of meeting industry needs for interoperable electrical channels.
  - OIF provides a forum where inputs come together from chip, connector, component, and equipment vendors.
  - The complete ecosystem benefits from the industry working together.
- Developing next generation 56 Gb/s electrical link technologies and standards will be more challenging than previous generations:
  - NRZ is not a viable technology for higher loss applications.
  - Substantial reductions in channel losses are not likely to occur.
  - Power consumption is becoming an overwhelming concern.
  - Power and I/O density of large ASICs is becoming constrained, causing system architecture changes and creating new interface applications.
- Competing technologies are emerging and cost-crossover may eventually occur:
  - Costs are dropping for optical backplane technologies.
  - If cost cross-over occurs, will substantially change system backplanes.
- OIF is moving forward with CEI-56G projects. We expect to adopt technical baseline text for most applications at the July meeting.